REMARKS

In the above referenced Office action, claims 15-20 were withdrawn from further consideration as being drawn to a non-elected species. Applicant's election without traverse of species 1 (claims 1-14) in the reply filed on 8/16/04 was acknowledged. As a result of the withdrawal of claims 15-20 from examination, claims 15-20 are cancelled from the instant application.

In the same Office action, claims 1-5 and 9 were rejected under 35 U.S.C. 102(e) as being anticipated by Kane et al.; dependent claims 6-8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kane et al.; and claims 10-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kane et al. in view of Fusegawa et al.

Applicant has reviewed the examiner's assertions in regard to the aforementioned rejections and found them to be substantially word for word the same as the assertions found in the Office action for claims 1-14 of the parent application Serial Number 10/056,199, now abandoned. However, the instant application is a Continuation-In-Part (CIP) of the '199 application. The claims in the instant application include significantly different limitations compared to the claims in the '199 application. As a result, Applicant respectfully submits that it was improper for the Examiner to reject the claims at issue for the same reasons used in the '199 application which is directed to a different invention.

Applicant contends that none of the claims 1-14 in the instant CIP application are anticipated by Kane et al. or are unpatentable over Kane et al. in view of Fusegawa et al.

Kane et al. is directed to a method of making a micro-mirror light beam switch using micro-fabrication or MEMS techniques. The preferred micro-fabrication method is disclosed in Kane et al. starting at col. 10, line 37 and continues over to col. 11, line 21 and includes ten steps. Kane et al. use Figures 2 through 11a to illustrate the ten micro-fabrication steps. In Kane's first step as shown in his Figure 2, a layer (8) of silicon nitride or silicon dioxide is deposited over a silicon wafer substrate (7) by chemical vapor deposition (CVD). The SiN or SiO_2 layer (8) will become the support member 5 as shown in Figure 1. The Kane method goes through a number of additional steps to form the piezo PZT actuators (11) about a central area on layer (8). Hinged areas (4) are formed between the PZT actuators (11) and central area on layer (8) as shown in Kane's Figure 9. In Kane's ninth step, the silicon wafer substrate (7) is etched from beneath the central area of layer (8) using deep reactive ion etching to create a free-floating

central area of layer (8) as shown in Figures 8 and 10. In Kane's last step, a mirror material (12) is deposited on support layer (8) in the central area using evaporation and lift-off patterning techniques to create the resultant optical switch as illustrated in Figure 11a. It is important to note that the mirror material (12) is not deposited on the silicon wafer substrate (7) which has been etched away, but rather on the support layer (8) which is the free-floating support member made of silicon nitride or silicon dioxide in step number one.

Fusegawa et al. do not add much substantive material to the teachings of Kane et al. Fusegawa et al. is directed to the processes of: pulling a single-crystal silicon wafer by the Czochralski (CZ) method, slicing a wafer from the ingot to a proper thickness; and preparing the wafer for integrated circuit applications. Fusegawa et al. is directed primarily to semiconductor wafer technology. None of the Fusegawa's processes are related to a mirror or the making thereof.

In contrast to these prior art techniques and products, independent claim 1 of the instant application recites a macroscopic mirror and independent claim 11 recites a method of making the same. In addition, claim 1 recites a silicon substrate of a predetermined shape and macroscopic size cut from a silicon wafer and independent claim 11 recites cutting a substrate section from the prepared silicon wafer to a predetermined shape and macroscopic size. Neither Kane et al. nor Fusegawa et al., taken individually or in combination, teach or suggest a macroscopic mirror or the manufacture thereof.

Applicant's specification goes to great lengths to distinguish the macroscopic mirror of the present invention from the microscopic mirrors of the cited prior art. Reference is made particularly to paragraphs 0008 to 0012 of the instant application. The cited references, including Kane et al., are directed to making micro-mirrors using micro-fabrication or MEMS techniques and refer to a large MEMS fabricated micro-mirror as being in the range of 200 μm x 200 μm to 2 mm x 2 mm (paragraph 0008). In paragraph 0010, it is stated that the Toshiyoshi et al. paper refers to a scanner micro-mirror of 400 μm x 400 μm x 30 μm which was considered in the paper to be a relatively large mirror at the microscopic scale. In comparison, Applicant's macroscopic mirror is on the order of 50 mm x 70 mm which is several orders of magnitude larger than a large micro-mirror of the cited prior art.

Applicant knows of no mirror of a macroscopic size having a substrate section cut from a silicon wafer. In paragraph 0003, Applicant states that known conventional macroscopic mirrors

for scanning applications have substrates commonly made from BK-7, Pyrex, Zerodur, Aluminum and the like. Desired specifications for a wide angle scanning application of a macroscopic mirror are set forth in paragraph 0004. In paragraphs 0005 - 0007, Applicant sets forth the problems associated with achieving these specifications with the commonly used materials of the prior art and in paragraph 0012 explains that the micro-fabrication techniques for producing microscopic mirrors cannot be extended to the manufacture of macroscopic mirrors of the desired specifications for wide angle scanning applications (see also paragraphs 0034 and 0035).

Claim 1 recites a plurality of layers, including a reflective medium, disposed on the flat, polished surface of the silicon substrate section in such a manner to minimize flexural distortion of the flat surface and independent claim 11 recites the step of applying the plurality of layers. Kane et al. do not teach or suggest depositing the reflective medium on the silicon wafer substrate, but rather Kane teaches depositing it on the central area of the support member. Note that Kane's silicon wafer substrate was etched away from the central area of the support member prior to the deposition of the mirror material. Accordingly, Kane et al. do not teach or suggest a mirror with a silicon wafer substrate section. Furthermore, Kane et al. do not teach or suggest a plurality of layers, but rather only a single layer.

Another limitation recited in claims 1 and 11 is that one side of the silicon wafer substrate section comprises an etched, rough surface. Claim 11 goes even further, stating that the silicon wafer substrate is prepared by etching the other side of the substrate to a predetermined roughness. Since Kane et al. do not teach or suggest a mirror substrate using a silicon wafer, they likewise do not teach or suggest that one side has an etched, rough surface.

Accordingly, for the above given reasons, independent claims 1 and 11 are considered novel and patentable over Kane et al. and Fusegawa et al., either taken individually or in combination.

Claims 2-10 are dependent from claim 1 and claims 12 -14 are dependent from claim 11. Each of these dependent claims include all of the limitations of their respective parent claims and therefore, are also considered novel and patentable over Kane et al. and Fusegawa et al. for the same reason given above for their parent claims.

In addition, there are limitations found in these dependent claims 2-10 and 12-14 of the instant CIP application that are distinguishable over Kane et al. and Fusegawa et al. in their own

right. For example, claim 5 recites that the plurality of layers comprise a bottom layer, a middle reflective medium layer, and a top protective coating layer, claim 6 is dependent from claim 5 and recites that each layer of the plurality of layers is applied by sputtering to a predetermined thickness; and claim 8 recites the substrate section is cut from the wafer in the form of an ellipse having a major axis dimension of approximately 70 mm and a minor axis dimension of approximately 50 mm. In addition, claim 12 recites that the substrate section is cut from the silicon wafer in a cookie cutter fashion, and claims 10 and 13 recite that the substrate section is laser cut from the silicon wafer. Moreover, claim 14 recites steps of applying the plurality of layers. Neither Kane et al. nor Fusegawa et al., taken individually or in combination, teach or suggest any of the aforementioned limitations.

None of the above mentioned limitations recited in claims 1-14 have been shown to be taught or suggested by Kane et al. and Fusegawa et al., either taken individually or in combination. Also, it has not been shown that what may be obvious to one of ordinary skill in the art for a microscopic sized mirror is also obvious for a macroscopic sized mirror, nor has it been shown that the micro-fabrication techniques used to make microscopic mirrors can be extended to make the claimed macroscopic mirror. Therefore, it is respectfully requested that the originally submitted claims 1-14 of the instant CIP application be re-examined and reconsidered for allowance based on the recitation thereof.

The prior art of record, which was not relied upon in the instant Office action, was considered not to affect the patentability of claims 1-14 for the same reasons given for Kane et al. and Fusegawa et al.

In view of the above, the claims 1-14 are considered allowable and the instant application considered in condition for allowance. Thus, it is respectfully solicited that the instant application be given an early issuance.

Respectfully submitted,

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